REMARKS

I. Status Summary

Claims 1-16 are pending in the present application. Claims 1, 3, and 5 have been amended. Claim 2 has been canceled. Therefore, upon entry of this Amendment, Claims 1 and 3-16 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Claim 1 has been amended to include the features of canceled Claim 2. Further, Claim 1 has been amended to place the claim in better method claim format. Support for the amendments to Claim 1 can be found throughout the present application, particularly at page 11, line 21, and Figure 2A.

II. Drawings

The Examiner stated that Figure 3 should be designated by a legend such as "Prior Art" because only that which is old is illustrated. (Official Action, page 2.) Figure 3 has been designated "PRIOR ART" in red ink in the revised drawings attached hereto. Therefore, applicants submit that Figure 3 has been properly labeled as prior art. Upon approval by the Examiner of the proposed drawing changes, formal drawings will be promptly submitted by applicants.

III. Claim Rejections Under 35 U.S.C. §§ 102 and 103

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by applicants' admitted prior art (AAPA). Claims 1-11 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,444,548 to Divakaruni et al.

(hereinafter, "Divakaruni"). Claims 12 and 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Divakaruni. These rejections are respectfully traversed.

Claim 1 recites a method for fabricating a semiconductor structure having a plurality of gate stacks on a semiconductor substrate. The method includes applying the gate stacks to a gate dielectric above the semiconductor substrate. Further, the method includes forming a sidewall oxide on sidewalls of the gate stacks. The method also includes applying and patterning a mask on the semiconductor structure. Further, the method includes implanting a contact doping in a self-aligned manner with respect to the sidewall oxide of the gate stacks in regions not covered by the mask. Claim 1 has been amended to recite, after implanting the contact doping, reducing the sidewall oxide in its lateral extent in regions not covered by the mask for resulting in a thinned sidewall oxide. Summarily, neither AAPA nor Divakaruni, alone or in combination, teaches or suggests reducing the sidewall oxide in its lateral extent in regions not covered by a mask for resulting in a thinned sidewall oxide, as recited by Claim 1.

AAPA is directed to a conventional planar semiconductor structure. Referring to Figure 3, the conventional planar semiconductor structure of AAPA includes a first gate stack **GS1** and a second gate stack **GS2** arranged on a semiconductor substrate **10** with a passivation layer **11** formed thereon. (Application, page 2, lines 21-25.) Gate stacks **GS1** and **GS2** also include a polysilicon structure **14** and a silicide layer **15**. (Application, page 2, lines 25-29.) Further, polysilicon structure **14** and a silicide layer **15** are provided with a sidewall oxide **17** at their sidewalls. Applicants respectfully

submit that AAPA does not disclose or suggest reducing the sidewall oxide in its lateral extent, as required by Claim 1.

Divakaruni fails to overcome the significant shortcomings of AAPA. The Examiner stated that the features of Claim 1 are disclosed in columns 3 and 4, and Figures 3 and 5A, of Divakaruni. Figure 3 of Divakaruni illustrates a deep trench capacitor **300**, a transistor **301** controlling access to deep trench capacitor **300**, and an opening **302** in which a bitline contact will be formed. (Divakaruni, column 3, lines 18-23.) Transistor **301** includes a gate conductor (GC) and a nitride cap (NIT) **304** which are bordered by insulating spacers **305**. (Divakaruni, column 3, lines 23-25.) Further, the structure is covered with an insulator such as boron phosphorous silicate glass (BPSG) **311** which includes an underlying insulator layer **312**. (Divakaruni, column 3, lines 31-34.) Divakaruni does not disclose or suggest reducing insulating spacer **305** in its lateral extent for resulting in a thinned sidewall oxide. Further, applicants respectfully submit that, in the Figure 3 embodiment of Divakaruni, there is no disclosure or suggestion of reducing a sidewall oxide in its lateral extent in regions not covered by a mask for resulting in a thinned sidewall oxide, as required by Claim 1.

Regarding the Figure 5A embodiment of Divakaruni, a photoresist **41** (Figure 4) is stripped and nitride barrier **50** is deposited on a GC/NIT gate stack including a sidewall. (Divakaruni, column 4, lines 58 and 59.) Nitride barrier **50** is deposited and structured on the semiconductor device using a unisotropical etch process in which the nitride layer on the sidewalls of the GC/NIT gate stack is thinned. (Divakaruni, column 4, line 58, to column 5, line 11.) Applicants respectfully submit that Divakaruni does

not disclose or suggest reducing the sidewall oxide in its lateral extent, as required by Claim 1.

The features recited by Claim 1 can be advantageous for several reasons. For example, referring to Figures 1A-2B, the reduction of the lateral extent of a sidewall oxide **17** for resulting in thinned sidewall oxide **17'** can enable a spatial separation of the halo implantation since the latter requires a lateral "lead" over the highly-doped section **13**. The effectiveness of p-doped section **18** (halo implant) is thereby increased. If the halo implantation is carried out at an angle α (differing from 0°), the thinning of sidewall oxide **17** to provide **17'** results in an increase in the possible angle α_{max} before complete shading occurs during the implantation as a result of the adjacent gate stack structure. The effectiveness of the halo implantation can also increase with a larger α. This technique may be carried out using a single photomask. Utilizing these techniques, it is possible to realize, for example, a selection transistor in the cell array of a DRAM with an extremely low connection resistance (on the source side).

Further, the features recited by Claim 1 can be advantageous for saving a mask or a resist plane in the fabrication process and also carrying out both a "single-sided halo implant" for the selection transistor in the cell array and the contact hole implantation for a CB contact with a single mask plane (GA plane). This combination of two implantations formerly with two required resist planes (GA plane and YA plane) to form a single plane (GA plane) makes it possible to realize, on the CB side, extremely low connection resistances or series resistances for the selection transistors in a cell array without jeopardizing or reducing the retention time of the cell signal.

Another advantage of the features recited by Claim 1 is that the n-type implantation is effected in a self-aligned manner with respect to the gate or with respect to the gate oxide and ensures an extremely low connection resistance of the selection transistor. Furthermore, an implantation through the finished CB contact hole can be provided since this n-type implantation provided in a self-aligned manner with respect to the gate edge ensures a low contact resistance of the CB contact. This can result in a complete photolithographic plane in, for example, 110 nm technology.

For the above reasons, Applicants respectfully submit that AAPA and Divakaruni neither teach nor suggest the features recited by Claim 1, and therefore that Claim 1 and its dependent claims are not obvious in view of the cited references. Applicants, therefore, respectfully request that the rejection of Claims 1 and 3-16 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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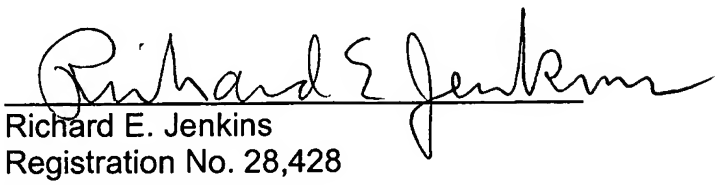
Date: May 26, 2005 By: 

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